CLAIMS

1. A skew correction apparatus for receiving a plurality of serial data through a plurality of channels and reducing the skew amount constituting a phase shift between a plurality of said serial data, comprising:

first skew correction means for detecting the skew between a plurality of said serial data during the idle time when no data is transmitted and correcting the delay amount of each of a plurality of said serial data in such a manner as to reduce said skew amount; and

second skew correction means for detecting the skew amount generated between a plurality of said serial data during the transmission of the data corrected by said first correction means and correcting the skew amount of each of a plurality of said serial data in such a manner as to reduce the skew amount to zero.

2. A skew correction apparatus according to claim 1,

wherein said first skew correction means includes an idle state detection circuit for detecting an idle state and a primary skew correction circuit for correcting the delay amount of each of a plurality of said serial data by the primary correction at the time of detecting said idle state, and

wherein said second skew correction means includes a skew monitor circuit for monitoring the skew amount during the transmission of a plurality of said serial data having a delay amount corrected by said primary skew correction circuit, and a delay adjust circuit for correcting the delay amount of each of a plurality of said serial data in such a manner that the skew amount detected by the skew monitor circuit is reduced to zero.

3. A skew correction apparatus according to claim 2,

wherein said primary skew correction circuit includes a select circuit for selecting one of a

plurality of said serial data and a delay amount control circuit for controlling the delay amount of the received serial data in such a manner as to minimize the phase difference between said selected serial data and each of a plurality of said serial data.

4. A skew correction apparatus according to claim 2,

wherein each of a plurality of said received serial data is configured with continuous bytes and includes additional information at the head of each of said bytes in addition to the transmission data;

wherein said skew monitor circuit includes:

a clock recovery circuit for extracting a bit clock for identifying the bits of reference serial data, a byte clock for identifying the byte of said reference serial data, an early clock changed later than the byte clock within the range of the timing width corresponding to the additional information contained in said reference serial data, and a delay clock changed later than said early clock within the range of the timing width corresponding to said additional information contained said reference serial data, said reference serial data being received through selected one of a plurality of said channels;

an additional information check circuit for determining whether the time of change of said early clock and the time of change of said delay clock are included or not in the timing width corresponding to said additional information contained in the serial data received through a channel other than said selected channel; and

a second delay adjust circuit for correcting the delay amount of the serial data of a corresponding channel in such a manner as to reduce the skew amount to zero in the case where it is determined that at least one of the time of change of said early

clock and the time of change of said delay clock is not contained in the receive timing width of said additional information contained in the serial data received by said additional information check circuit through a channel other than said selected channel.

5. A skew correction apparatus according to claim 4:

wherein said additional information is one-bit information having "1" and "0" alternating for each of the continuous bytes;

wherein said additional information check circuit includes, for each channel,

a first latch circuit for outputting a first latch signal which assumes a first state in the case where the serial data is "1" and assumes a second state different from the first state in the case where the serial data is "0" at the time of change of said early clock;

a second latch circuit for outputting a second latch signal which assumes a first state in the case where the serial data is "1" and assumes a second state different from the first state in the case where the serial data is "0" at the time of change of said delay clock;

a first determination circuit for determining whether the output of said first latch circuit deviates from the alternating pattern of "1" and "0" over a predetermined number of bytes; and

a second determination circuit for determining whether the output of the second latch circuit deviates from the alternating pattern of "1" and "0" over a predetermined number of bytes; and

wherein said second delay adjust circuit includes a variable delay circuit for adjusting, for each channel, the delay amount in such a manner as to advance the phase of the serial data of said channel with respect to said reference serial data in the case where the

output of said first determination circuit deviates from the alternating pattern of "1" and "0" over a predetermined number of bytes, and adjusting, for each channel, the delay amount in such a manner as to retard the phase of the serial data of said channel with respect to said reference serial data in the case where the output of said second determination circuit deviates from the alternating pattern of "1" and "0" over a predetermined number of bytes.

6. A skew correction apparatus according to claim 2,

wherein each of a plurality of said received serial data is configured with continuous bytes;

wherein said skew amount monitor circuit includes:

a reference channel clock recovery circuit for extracting a reference byte clock for identifying the bytes of the reference serial data received through selected one of a plurality of said channels;

at least one normal channel clock recovery circuit for extracting a normal byte clock for identifying the bytes of the serial data received through a channel other than said selected channel;

a phase comparator/voltage conversion circuit for detecting the phase difference between the phase of the byte clock extracted by said normal channel clock recovery circuit and the phase of said byte clock extracted by said reference channel clock recovery circuit, and converting said phase difference into a voltage value; and

a second delay adjust circuit for correcting the delay amount of the serial data of a corresponding channel in such a manner as to reduce the skew amount to zero in accordance with the the voltage value.